REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-11, 20-25, and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art or, alternatively, U.S. Patent 5,561,628 to Terada et al. ("Terada").

Claims 1-11, 20-25, and 30 have been canceled without prejudice. New claims 31-37 have been added.

Support for new claims 31-37 is found in the specification at pages 9-15 and in Figure 3 of the drawings and in the originally filed claims 1-11.

It is respectfully submitted that in view of the above-listed support, new claims 31-37 do not add new matter.

The Examiner has rejected claims 1-11, 20-25, and 30 under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art or, alternatively, Terada. In particular, the Examiner states:

> Claims 1-11 and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' prior art or, alternatively, Terada *et al* (5,561,628). Applicants admit that it was known to include a status register in a memory device, including one wherein the status register includes at least one bit to indicate the suspension of an erase operation, namely ESS. The Terada reference also teaches the status registers. Further, applicants discuss the relative time requirements for erase operations, programming (writing) operations and reading operations. These timings were also well known in the art. At the time of the Terada application (1994), popular microprocessor speeds were on the order of 90-100 MHZ. Recently, microprocessor speeds of 450 MH'Z have been announced. The faster the processor, the greater the adverse impact of a fixed delay, such as the latency for a flash memory write. At 450 MHZ, a fixed latency impacts about 4 1/2 times as many clock cycles as it did at 100 MHZ. Therefore, in view of the continually increasing processor speeds, it would have

been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have provided for means to suspend the programing of a flash memory to serve other requests because of the tremendous impact that latency would have on the more recent processors and the applications running on those processors. It appears that the other claimed elements to support the write operation suspend status bit are equivalent to the support elements required for support of the prior art ESS bit, and it would therefore have been obvious to include such support elements.

(1/6/99 Office Action, pp. 2-3).

Applicants respectfully submit, however, that new claim 31 is not obvious under 35 U.S.C. § 103(a) in view of applicants' admitted prior art or Terada. New claim 31 includes the limitations of:

> A memory device, comprising:
> a memory array;
> a register configured to store at least one bit indicating a suspend status of a write operation; and
> a control circuit coupled to said memory array and said register, said control circuit is configured to update said register and to control the output of a status signal representing said protection status of said data modification operation, and wherein said control circuit includes:
> a first state machine configured to update at least one of said bits indicating said suspend status of said write operation in response to a suspend signal, and
> a second state machine coupled to said first state machine and configured to control the output of said status signal in response to a status request signal.

(Claim 31)(emphasis added).

In contrast to claim 31, neither applicants' admitted prior art nor Terada disclose or suggest a register configured to store at least one bit indicating a suspend status of a write operation.

In further contrast to claim 31, neither applicants' admitted prior art nor Terada disclose or suggest a first state machine configured to update at least one of said bits indicating said suspend status of said write operation in response to a suspend signal.

In still further contrast to claim 31, neither applicants' admitted prior art nor Terada disclose or suggest a second state machine coupled to said first state machine and configured to control the output of said status signal in response to a status request signal.

In the specification, a prior art status register is described with reference to Figure 1. In particular, the specification discloses:

> Figure 1 illustrates one embodiment of a status register for a prior art flash memory device that is capable of performing programming, erase, and read operations. The status register 100 includes the five memory locations 101 through 105 with each memory location storing at least one memory bit . . . memory location 101 stores Vpp status ("VPPS") information; the memory location 102 stores byte write and set lock bit status ("BWSLBS") information; the memory location 103 stores erase and clear lock bits ("ECLBS") information; the memory location 104 stores erase suspend status ("ESS") information; and the memory location 105 stores write state machine status ("WSMS") information.

(p. 2 Specification).

Terada discloses that:

> Each of the lash memories 40a to 40d includes a status register 41 in which values of registers SR.0 to SR.7, corresponding to bit 0 to bit 7, vary depending on the operation state of the memory. The data stored in the status register 41 can be read to the outside of the PC card 100 via a data bus for transmitting data signal D0 to D15.
>
> The arrangement of the registers SR.0 to SR.7 of the status register 41 is described in Table 1 below. The meanings of the registers SR.0 to SR.7 are described in Table 2.

As such, applicants' admitted prior art and Table 2 of Terada do not disclose the status register, first state machine, and second state machine as recited in claim 31, therefore, claim 31 is not obvious under § 103(a) over applicants' admitted prior art and Terada and is in condition of allowance.

Given that claims 32-37 depend directly or indirectly on claim 31, applicants submit that new claims 32-37 are not obvious under § 103(a) over applicants' admitted prior art and Terada and are in condition of allowance.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome.

If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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